

"FEE ADDRESS" INDICATION FORM

To: MAIL STOP: M Fee Correspondence
U.S. Patent & Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

Please recognize as the "Fee Address," under the provisions of 37 CFR 1.363, the following address:

COMPUTER PATENT ANNUITIES, INC.
225 Reinekers Lane
Suite 400
Alexandria, VA 22314

Payor Number: 000197

in the following listed application(s) or patent(s) for which the issue fee has been paid.

<u>Patent No.</u>	<u>Serial No.</u>	<u>Patent Date</u>	<u>US Filing Date</u>	<u>Confirmation No.</u>	<u>Attorney Docket No.</u>
7,187,204 B2	10/807,692	03/06/2007	03/24/2004	4403	0553-0401

Respectfully Submitted,



Mark J. Murphy
Registration No. 34,225
Date: May 5, 2008

COOK, ALEX, McFARRON,
MANZO, CUMMINGS & MEHLER, Ltd.
200 West Adams Street
Suite 2850
Chicago, Illinois 60606
(312) 236-8500

Customer No: 26568



US007187204B2

(12) **United States Patent**
Tanada

(10) **Patent No.:** **US 7,187,204 B2**
(45) **Date of Patent:** **Mar. 6, 2007**

(54) **CIRCUIT FOR INSPECTING
SEMICONDUCTOR DEVICE AND
INSPECTING METHOD**

(75) Inventor: **Yoshifumi Tanada, Atsugi (JP)**

(73) Assignee: **Semiconductor Energy Laboratory
Co., Ltd. (JP)**

(*) Notice: Subject to any disclaimer, the term of this
patent is extended or adjusted under 35
U.S.C. 154(b) by 36 days.

(21) Appl. No.: **10/807,692**

(22) Filed: **Mar. 24, 2004**

(65) **Prior Publication Data**
US 2005/0035805 A1 Feb. 17, 2005

(30) **Foreign Application Priority Data**

Mar. 25, 2003 (JP) 2003-081666
May 15, 2003 (JP) 2003-137822

(51) **Int. Cl.**
H03K 19/21 (2006.01)
G06K 7/50 (2006.01)

(52) **U.S. Cl.** **326/52; 326/54; 326/9;
345/84**

(58) **Field of Classification Search** **326/9,
326/11-14, 52, 54; 345/92, 104**
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,775,891 A * 10/1988 Aoki et al. 348/572
5,068,547 A * 11/1991 Gascoyne 326/16
5,410,247 A * 4/1995 Ishizuka 324/158.1
5,825,204 A * 10/1998 Hashimoto 326/54
6,455,336 B1 * 9/2002 Berndlmaier et al. 438/14
6,573,774 B1 * 6/2003 Gardner 327/201
6,711,041 B2 * 3/2004 Pereira et al. 365/49
6,762,617 B2 * 7/2004 Iwase et al. 326/11

6,762,735 B2 7/2004 Koyama 345/76
6,850,080 B2 2/2005 Hiroki 324/750
2001/0035526 A1 11/2001 Yamazaki et al. 257/57
2001/0040565 A1 11/2001 Koyama 345/204
2002/0130675 A1 9/2002 Hiroki 324/750
2002/0132383 A1 9/2002 Hiroki et al. 438/17
2004/0119824 A1 6/2004 Osada 348/180

(Continued)

FOREIGN PATENT DOCUMENTS

JP 05-256914 10/1993

(Continued)

OTHER PUBLICATIONS

International Search Report for application No. PCT/JP2004/
003549, dated Apr. 27, 2004 (In Japanese).

(Continued)

Primary Examiner—Vibol Tan

(74) *Attorney, Agent, or Firm*—Cook, Alex, McFarron,
Manzo, Cummings & Mehler, Ltd.

(57) **ABSTRACT**

It is configured by plurality of NAND circuits connected in series through a plurality of inverters, and a plurality of NOR circuits connected in series through the plurality of inverters. Each of a plurality of source signal lines provided in a pixel portion is connected to one input terminal of a NAND circuit and a NOR circuit, and an output of an inspection is obtained from final lines of the NAND circuit and the NOR circuit connected in series. In this manner, an inspecting circuit which is capable of determining a defect simply and accurately by using a small-scale circuit, and a method thereof are provided.

25 Claims, 17 Drawing Sheets

